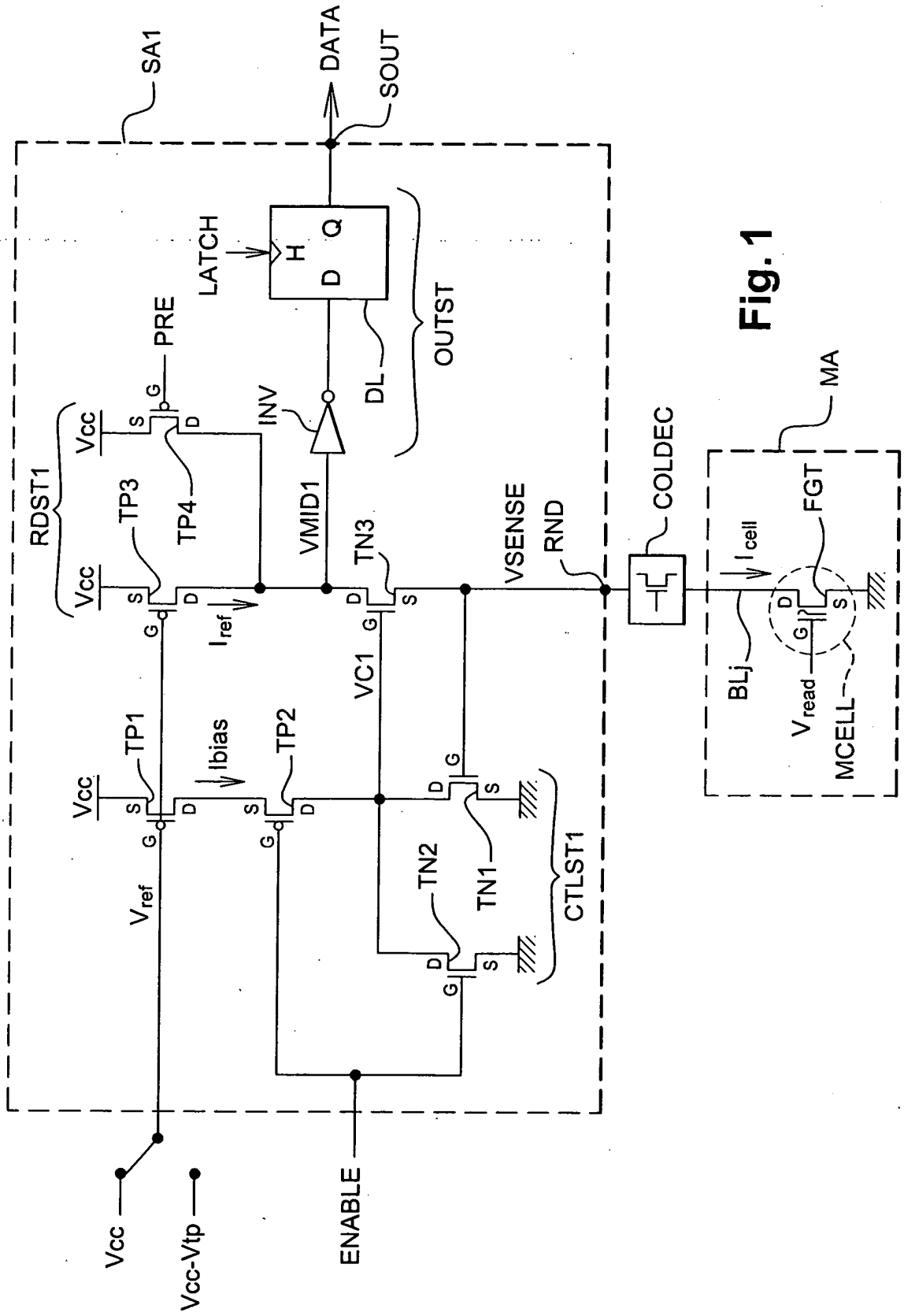

SA1
DATA
SOUT
LATCH
H
Q
D
OUTST
DL
PRE
INV
Vcc
RDST1
TP3
TP4
VMID1
TN3
VSENSE
RND
COLDEC
MA
FGT
Icell
BLj
Vread
MCELL
Iref
VC1
TP1
Ibias
TP2
Vref
TN2
TN1
CTLST1
Vcc
Vcc-Vtp
ENABLE

Fig. 1

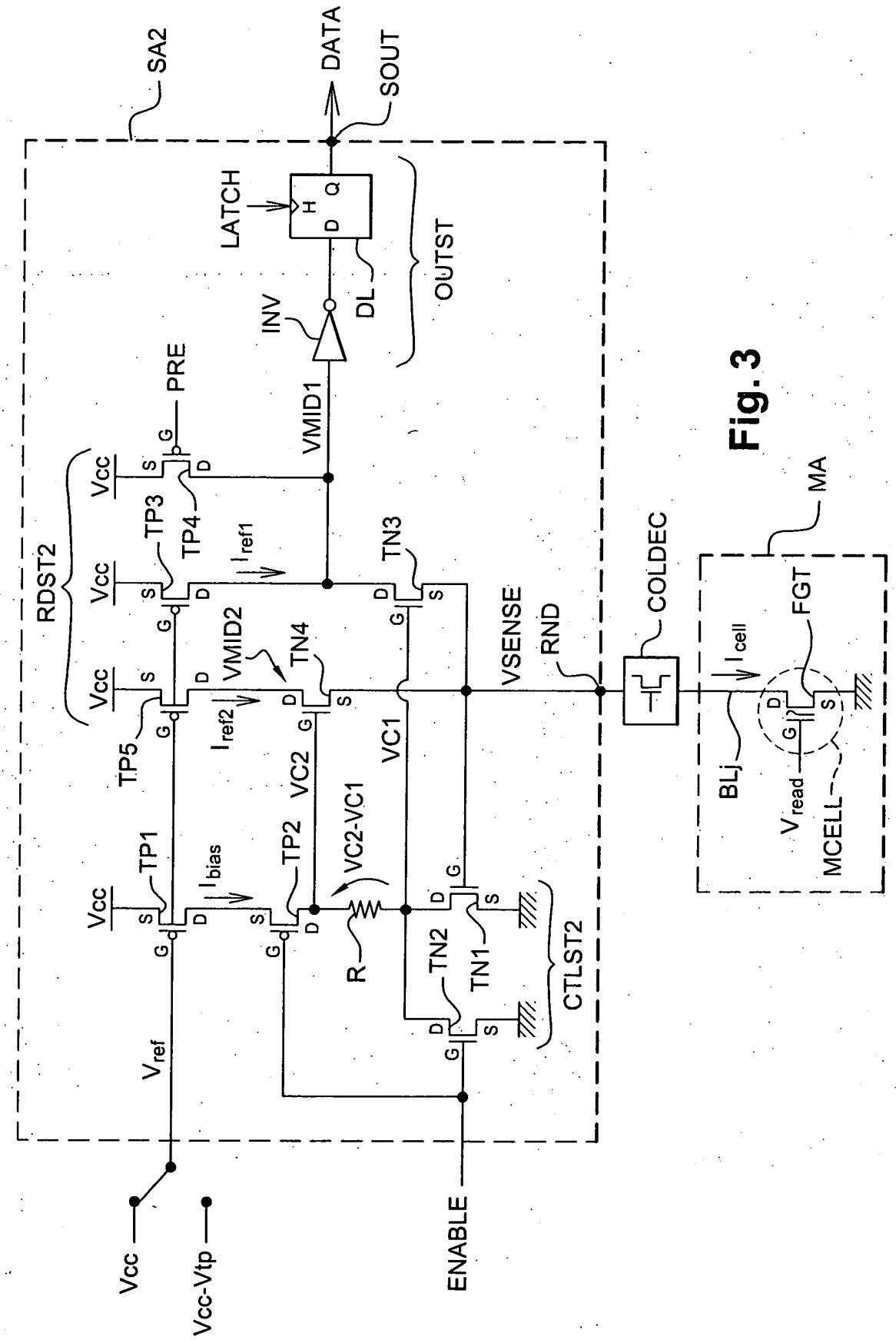

SA2
DATA
SOUT
LATCH
H
Q
D
DL
OUTST
INV
VMID1
PRE
G
S
D
Vcc
TP3
TP4
$I_{ref1}$
TN3
RDST2
VMID2
TN4
VSENSE
RND
COLDEC
MA
FGT
$I_{cell}$
BLj
$V_{read}$
MCELL
TP5
$I_{ref2}$
VC2
VC1
TP1
$I_{bias}$
TP2
VC2-VC1
R
TN2
TN1
CTLST2
$V_{ref}$
Vcc
Vcc-Vtp
ENABLE

Fig. 3

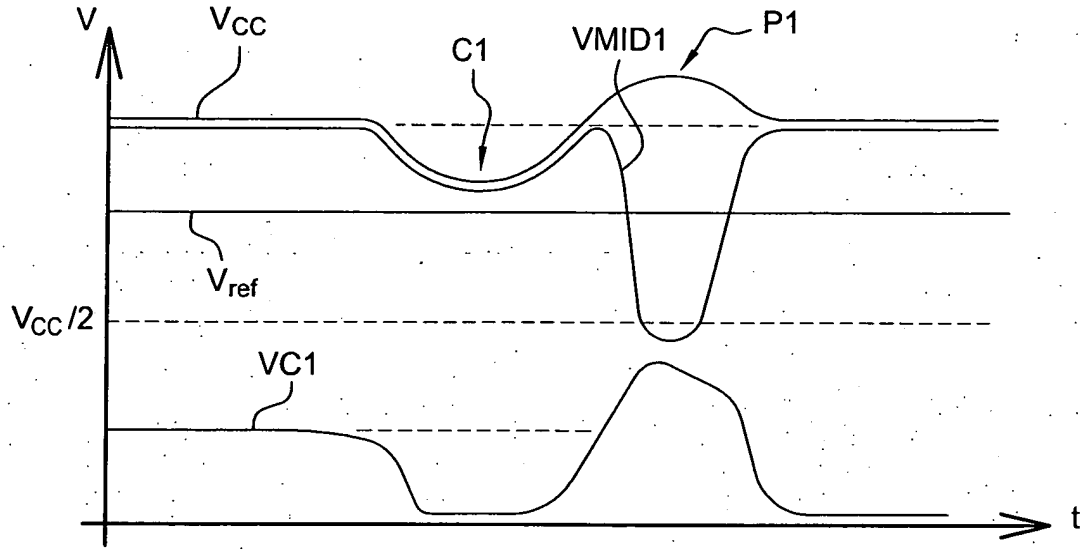

V
$V_{CC}$
C1
VMID1
P1
$V_{ref}$
$V_{CC}/2$
VC1
t

Fig. 2

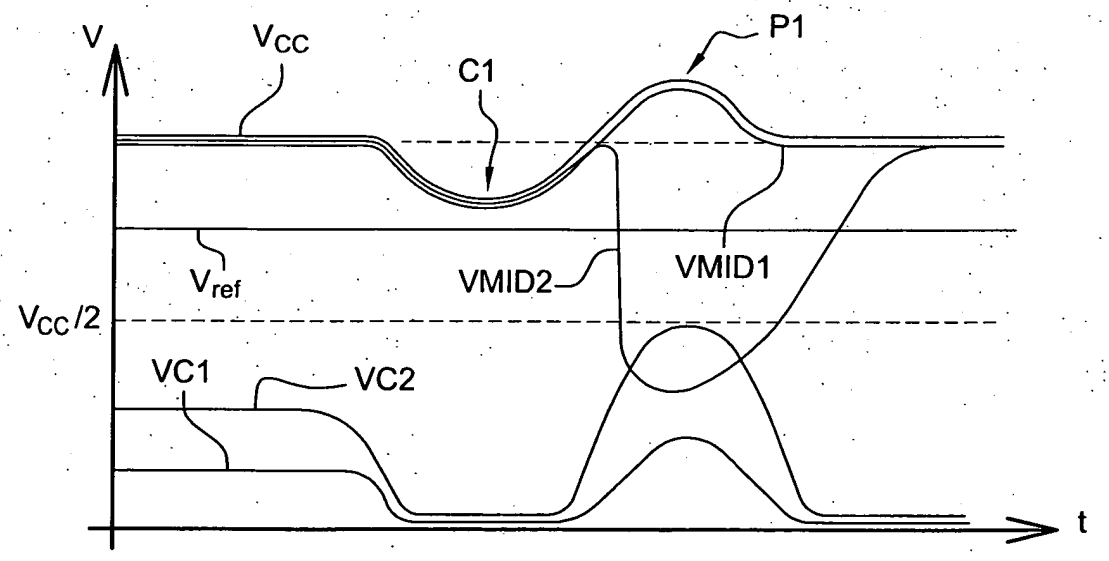

V
$V_{CC}$
C1
P1
$V_{ref}$
VMID2
VMID1
$V_{CC}/2$
VC1
VC2
t

Fig. 4

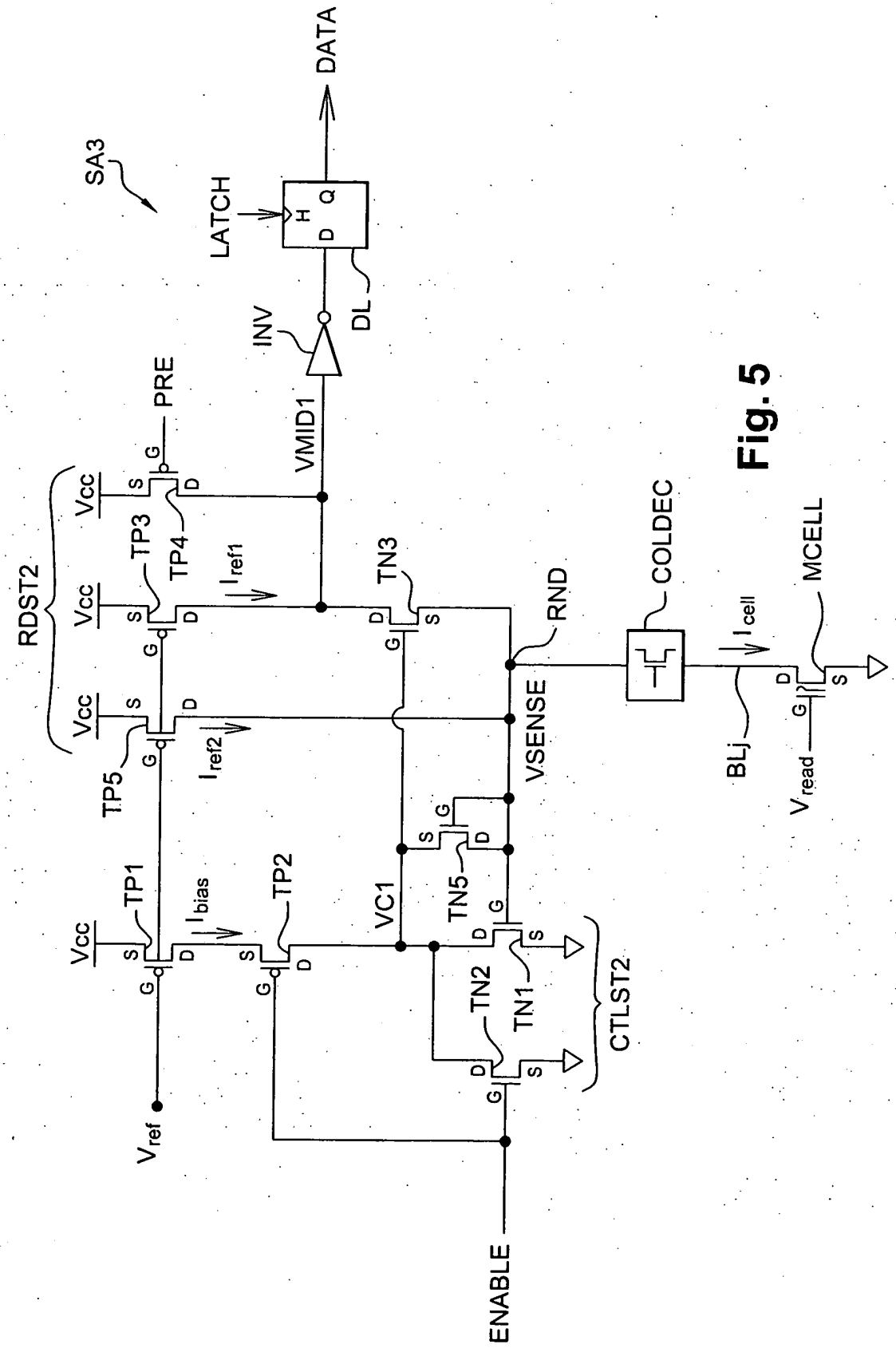

SA3
LATCH
H
Q
D
DATA
DL
INV
VMID1
PRE
Vcc
TP3
TP4
RDST2
$I_{ref1}$
TN3
RND
COLDEC
$I_{cell}$
MCELL
TP5
$I_{ref2}$
VSENSE
BLj
$V_{read}$
TP1
$I_{bias}$
TP2
VC1
TN5
TN2
TN1
CTLST2
$V_{ref}$
ENABLE
S
D
G

Fig. 5